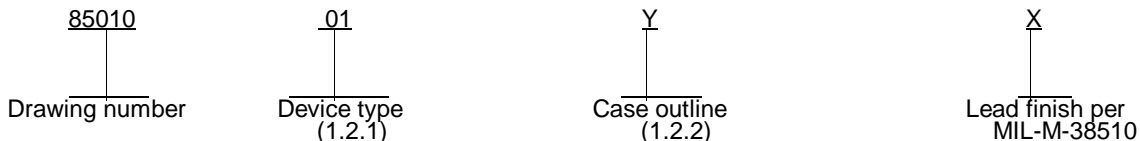


REVISIONS																						
LTR	DESCRIPTION										DATE (YR-MO-DA)				APPROVED							
C	Convert drawing to new boiler plate. Corrected vendor similar part number for vendor CAGE 34335. Editorial changes throughout.										90 Feb 6				W.Heckman							
<div>CURRENT CAGE CODE 67268</div>																						
REV	C	C	C	C																		
SHEET	35	36	37	38																		
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34		
REV STATUS OF SHEET				REV		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14			
PMIC N/A				PREPARED BY Jeffery Tunstall						DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444												
<div>STANDARDIZED MILITARY DRAWING</div> <div>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</div> <div>AMSC N/A</div>				CHECKED BY Tim H. Noh																		
				APPROVED BY William K. Heckman																		
				DRAWING APPROVAL DATE 18 OCTOBER 1985																		
				REVISION LEVEL  C						SIZE A	CAGE CODE <b>14933</b>	85010										
										SHEET		1	OF		38							

# 1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit
1	M80186	8 Mhz	16-bitN-channelmicroprocessor
02	M80186	6 Mhz	16-bit N-channel microprocessor

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Y	68-terminal ceramic quad package (see figure 1)
Z	P-AC (1.160" X 1.160"), pin grid array package

## 1.3 Absolute maximum ratings.

Voltage on any pin (referenced to GND) - - - - -	-1.0 V dc to +7.0 V dc
Storage temperature range- - - - -	-65° C to +150° C
Maximum power dissipation (P <sub>D</sub> ) - - - - -	-3 W
Thermal resistance, junction-to-case (O <sub>JC</sub> ):	
Case Y - - - - -	12° C/W
Case Z - - - - -	See MIL-M-38510, appendix C
Junction temperature (T <sub>J</sub> ) - - - - -	+150° C
Lead temperature (soldering, 5 seconds)- - - - -	+260° C

## 1.4 Recommended operating conditions.

Supply voltage range (V <sub>CC</sub> ):	
Device type 01 - - - - -	4.75 V dc to 5.25 V dc
Device type 02 - - - - -	4.75 V dc to 5.25 V dc
Frequency of operation:	
Device type 01 - - - - -	8 MHz
Device type 02 - - - - -	6 MHz
Case operating temperature range (T <sub>C</sub> ) - - - - -	-55° C to +125° C

**STANDARDIZED  
MILITARY DRAWING**  
 DEFENSE ELECTRONICS SUPPLY CENTER  
 DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
 C

SHEET  
 2

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

### SPECIFICATION

#### MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

### STANDARD

#### MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

### BULLETIN

#### MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-85010
		REVISION LEVEL C	SHEET 3

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ $V_{CC} = 5.0 \text{ V} \pm 5\%$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Low-level input voltage	$V_{IL}$		01, 02	1,2,3	-0.5		V
High-level input voltage (All except X1 and (RES))	$V_{IH1}$		01, 02	1,2,3	2.0	$V_{CC} + 0.5$	V
High-level input voltage at (RES)	$V_{IH2}$		01, 02	1,2,3	3.0	$V_{CC} + 0.5$	V
Low-level output voltage	$V_{OL}$	$I_{OL} = 2.5 \text{ mA}$ for $\overline{SO-S2}$ $I_{OL} = 2.0 \text{ mA}$ for all other outputs	01, 02	1,2,3		0.45	V
High-level output voltage	$V_{OH}$	$I_{OH} = -400 \mu\text{A}$	01, 02	1,2,3	2.4		V
Power supply current	$I_{CC}$	$V_{CC} = 5.25 \text{ V}$	01, 02	1,2,3		600	mA
Input leakage current	$I_{IL}$	$0 \text{ V} < V_{IN} < V_{CC}$	01, 02	1,2,3		$\pm 10$	$\mu\text{A}$
Output leakage current	$I_{OL}$	$0.45 \text{ V} < V_{OUT} < V_{CC}$	01, 02	1,2,3		$\pm 10$	$\mu\text{A}$
Low-level clock output voltage	$V_{CLO}$	$I_O = 4.0 \text{ mA}$	01, 02	1,2,3		0.6	V
High-level clock output voltage	$V_{CHO}$	$I_O = -200 \mu\text{A}$	01, 02	1,2,3	4.0		V
Low-level clock input voltage	$V_{CL1}$		01, 02	1,2,3	-0.5	+0.6	V
High-level clock input voltage	$V_{CH1}$		01, 02	1,2,3	3.9	$V_{CC} + 1.0$	V
Functional tests		See 4.3.1d	01, 02	7,8			
Input capacitance	$C_{IN}$	See 4.3.1c	01, 02			10	pF
I/O capacitance	$C_{IO}$	See 4.3.1c	01, 02			20	pF

See footnotes at end of table.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
4

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>CC</sub> = 5.0 V ±5% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Data in setup (A/D)	t <sub>DVCL</sub>	C <sub>L</sub> = 20 to 200 pF, all outputs	01,02	9,10,11	20		ns
Data in hold (A/D)	t <sub>CLDX</sub>		01,02	9,10,11	10		ns
Asynchronous ready (ALREADY) active setup time	t <sub>ARYHCH</sub>		01,02	9,10,11	20		ns
AREADY inactive setup time	t <sub>ARYLCL</sub>		01,02	9,10,11	38		ns
AREADY hold time	t <sub>CHARYX</sub>		01,02	9,10,11	15		ns
Synchronous ready (SREADY) transition setup time	t <sub>SRYCL</sub>		01,02	9,10,11	35		ns
SREADY transition hold time	t <sub>CLSRY</sub>		01,02	9,10,11	15		ns
Hold setup 2/	t <sub>HVCL</sub>		01,02	9,10,11	25		ns
INTR, NMI, TEST, TIMERIN setup 2/	t <sub>INVCH</sub>		01,02	9,10,11	25		ns
DRQ0, DRQ1, setup	t <sub>INVCL</sub>		01,02	9,10,11	25		ns
Address valid delay	t <sub>CLAX</sub>		01	9,10,11	5	59	ns
			02	9,10,11	5	63	ns
Address hold	t <sub>CLAX</sub>		01	9,10,11	5		ns
			02	9,10,11	5		ns
Address float delay	t <sub>CLAZ</sub>		01	9,10,11	t <sub>CLAX</sub>	35	ns
			02	9,10,11	t <sub>CLAX</sub>	44	ns
Address valid to clock high	t <sub>AVCH</sub>	01,02	9,10,11	10		ns	

See footnotes at end of table.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
5

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>CC</sub> = 5.0 V ±5% unless otherwise specified	Device type	Group A subgroups	Limits		Unit	
					Min	Max		
Command lines float delay	t <sub>CHCZ</sub>	C <sub>L</sub> = 20 to 200 pF, all outputs	01	9,10,11		45	ns	
			02	9,10,11		56	ns	
Command lines valid delay (after float)	t <sub>CHCV</sub>		01	9,10,11		55	ns	
			02	9,10,11		76	ns	
ALE width	t <sub>LHLL</sub>		01,02	9,10,11	t <sub>CLCL</sub> -35		ns	
ALE active delay	t <sub>CHLL</sub>		01	9,10,11		35	ns	
			02	9,10,11		44	ns	
ALE inactive delay	t <sub>CHLL</sub>		01	9,10,11		35	ns	
			02	9,10,11		44	ns	
Address hold to ALE inactive	t <sub>LLAX</sub>		01	9,10,11	t <sub>CHCL</sub> -25		ns	
			02	9,10,11	t <sub>CHCL</sub> -30		ns	
Data valid delay	t <sub>CLDV</sub>		01	9,10,11	5	44	ns	
			02	9,10,11	5	55	ns	
Data hold time	t <sub>CLDOX</sub>		01,02	9,10,11	5		ns	
Data hold after WR	t <sub>WHDX</sub>		01	9,10,11	t <sub>CLCL</sub> -40		ns	
			02	9,10,11	t <sub>CLCL</sub> -50		ns	
Control active delay 1	t <sub>CVCTV</sub>		01	9,10,11	5	70	ns	
			02	9,10,11	5	87	ns	
Control active delay 2	t <sub>CHCTV</sub>		01	9,10,11	5	73	ns	
			02	9,10,11	5	76	ns	
DEN inactive delay (non-write cycle)	t <sub>CVDEX</sub>		01	9,10,11	10	70	ns	
			02	9,10,11	10	87	ns	

See footnotes at end of table.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
6

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ $V_{CC} = 5.0\text{ V} \pm 5\%$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Address float to $\overline{\text{RD}}$ active	$t_{\text{AZRL}}$	$C_L = 20$ to $200\text{ pF}$ , all outputs	01,02	9,10,11	0		ns
$\overline{\text{RD}}$ active delay	$t_{\text{CLRL}}$		01	9,10,11	10	70	ns
			02	9,10,11	10	87	ns
$\overline{\text{RD}}$ inactive delay	$t_{\text{CLRH}}$		01	9,10,11	10	55	ns
			02	9,10,11	10	76	ns
$\overline{\text{RD}}$ inactive to address active	$t_{\text{RHAV}}$		01	9,10,11	$t_{\text{CLCL}}$ -40		ns
			02	9,10,11	$t_{\text{CLCL}}$ -50		ns
HLDA valid delay	$t_{\text{CLHAV}}$		01,02	9,10,11	5	67	ns
$\overline{\text{RD}}$ width	$t_{\text{RLRH}}$		01,02	9,10,11	$2t_{\text{CLCL}}$ -50		ns
$\overline{\text{WR}}$	$t_{\text{WLWH}}$		01,02	9,10,11	$2t_{\text{CLCL}}$ -40		ns
Address valid to ALE low	$t_{\text{AVAL}}$		01	9,10,11	$t_{\text{CLCH}}$ -25		ns
			02	9,10,11	$t_{\text{CLCH}}$ -45		ns
Status active delay	$t_{\text{CHSV}}$		01	9,10,11	10	55	ns
			02	9,10,11	10	76	ns
Status inactive delay	$t_{\text{CLSH}}$		01	9,10,11	10	65	ns
			02	9,10,11	10	76	ns
Timer output delay	$t_{\text{CLTMV}}$	$C_L = 100\text{ pF}$ maximum	01	9,10,11		60	ns
			02	9,10,11		75	ns
Control inactive delay	$t_{\text{CVCTX}}$	$C_L = 20$ to $200\text{ pF}$ , all outputs	01	9,10,11		55	ns
			02	9,10,11		76	ns

See footnotes at end of table.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
7

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>CC</sub> = 5.0 V ±5% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Reset delay	t <sub>CLRO</sub>	C <sub>L</sub> = 20 to 200 pF, all outputs	01	9,10,11		60	ns
			02	9,10,11		75	ns
Queue status delay	t <sub>CHQSV</sub>		01	9,10,11		35	ns
			02	9,10,11		44	ns
Chip-select active delay	t <sub>CLCSV</sub>		01	9,10,11	5	66	ns
			02	9,10,11	5	80	ns
Chip-select hold from command inactive	t <sub>CXCSX</sub>		01,02	9,10,11	35		ns
Chip-select inactive delay	t <sub>CHCSX</sub>		01,02	9,10,11	5	47	ns
CLKIN period	t <sub>CKIN</sub>		01	9,10,11	62.5	250	ns
			02	9,10,11	83	250	ns
CLKIN fall time	t <sub>CKHL</sub>	3.5 V to 1.0 V <u>3/</u>	01,02	9,10,11		10	ns
CLKIN rise time	t <sub>CKLH</sub>	1.0 V to 3.5 V <u>3/</u>	01,02	9,10,11		10	ns
CLKIN low time	t <sub>CLCK</sub>	1.5 V <u>3/</u>	01	9,10,11	25		ns
			02	9,10,11	33		ns
CLKIN high time	t <sub>CHCK</sub>	1.5 V <u>3/</u>	01	9,10,11	25		ns
			02	9,10,11	33		ns
CLKIN to CLKOUT skew	t <sub>CICO</sub>	C <sub>L</sub> = 20 to 200 pF, all outputs	01	9,10,11		50	ns
			02	9,10,11		62.5	ns
CLKOUT period	t <sub>CLCL</sub>		01	9,10,11	125	500	ns
			02	9,10,11	167	500	ns
CLKOUT low time	t <sub>CLCH</sub>	1.5 V <u>3/</u>	01,02	9,10,11	1/2 t <sub>CLCL</sub> -7.5		ns

See footnotes at end of table.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
8

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>C</sub> ≤ +125°C V <sub>CC</sub> = 5.0 V ±5% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
CLKOUT high time	t <sub>CHCL</sub>	1.5 V <u>3/</u>	01,02	9,10,11	1/2 t <sub>CLCL</sub> -7.5		ns
CLKOUT rise time	t <sub>CH1CH2</sub>	1.0 V to 3.5 V <u>3/</u>	01,02	9,10,11		15	ns
CLKOUT fall time	t <sub>CL2CL1</sub>	3.5 V to 1.0 V <u>3/</u>	01,02	9,10,11		15	ns

1/ All ac parameters tested as per circuit on figure 4.

2/ Setup requirements only to guarantee recognition at next CLK.

3/ Voltage indicated refer to voltage measurements on waveforms in figure 4.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
9

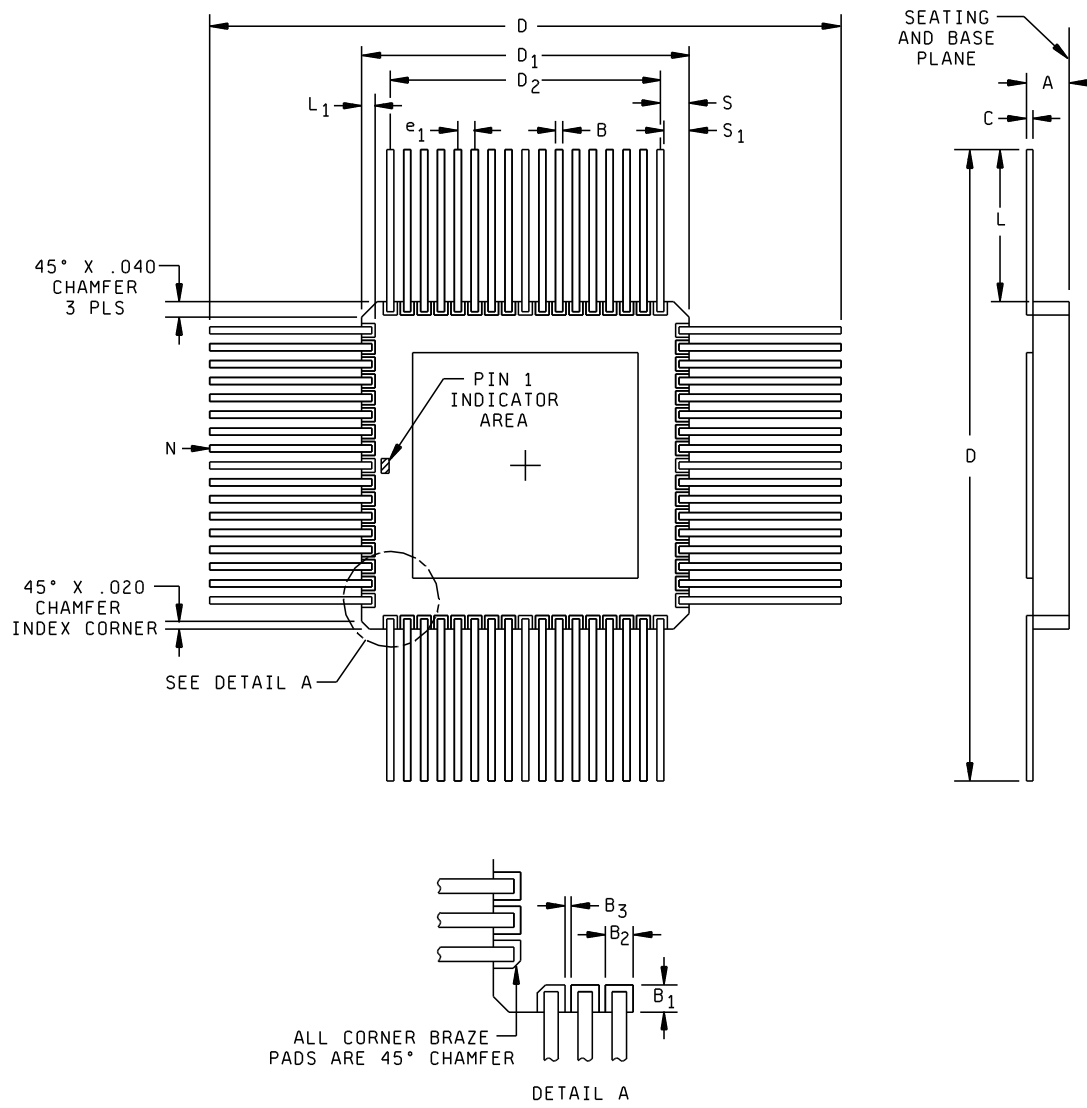


FIGURE 1. Case outline Y.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
10

Dimensions				
Ltr	Inches		Millimeters	
	Min	Max	Min	Max
A	.080	.106	2.03	2.69
B	.016	.020	0.41	0.51
B <sub>1</sub>	.040	.060	1.02	1.52
B <sub>2</sub>	.030	.040	0.76	1.02
B <sub>3</sub>	.005	.020	0.13	0.51
C	.008	.012	0.20	0.30
D	1.640	1.870	41.66	47.50
D <sub>1</sub>	.935	.970	23.75	24.64
D <sub>2</sub>	.800 BSC		20.32 BSC	
e <sub>1</sub>	.050 BSC		1.27 BSC	
L	.375	.450	9.53	11.43
L <sub>1</sub>	.040	.060	1.02	1.52
N	68 PINS		68 PINS	
S	.66	.087	1.68	2.21
S <sub>1</sub>	.050		1.27	

FIGURE 1. Case outline Y - Continued.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
11

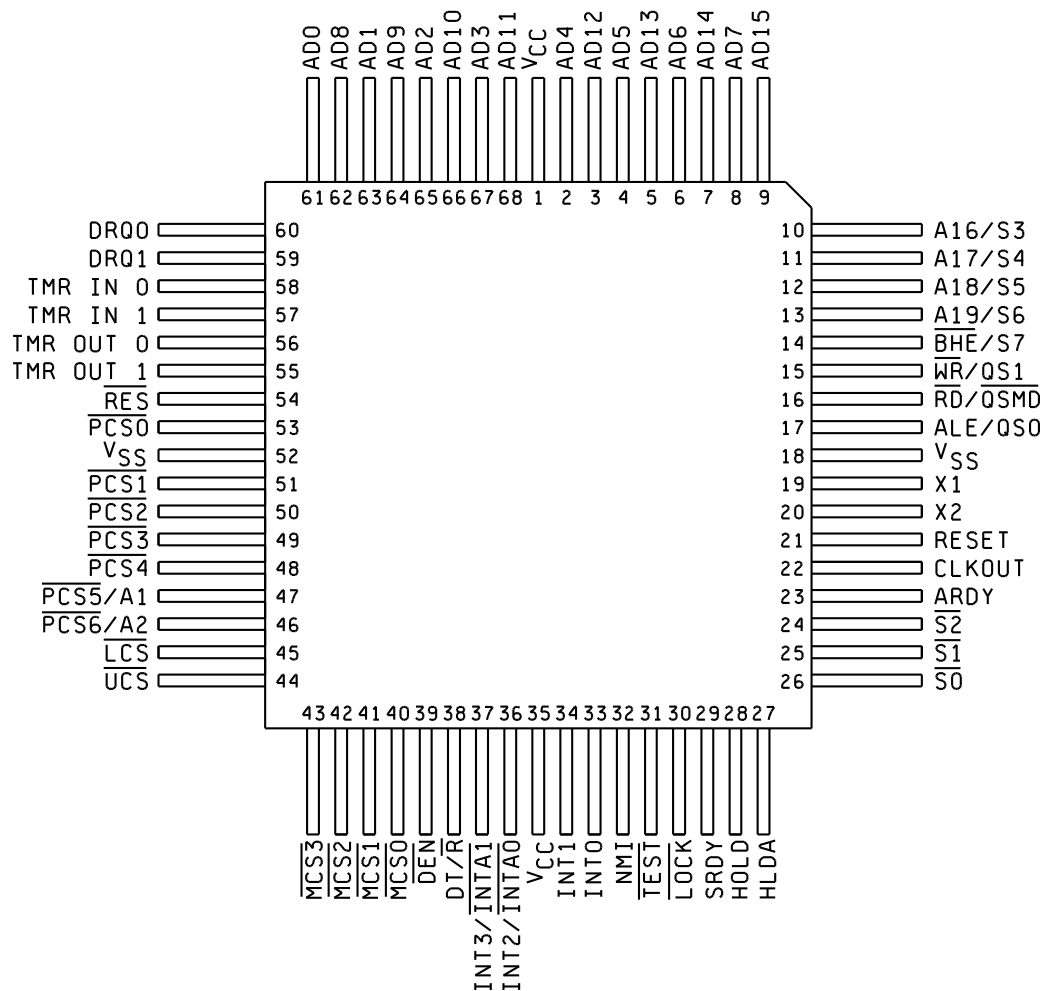
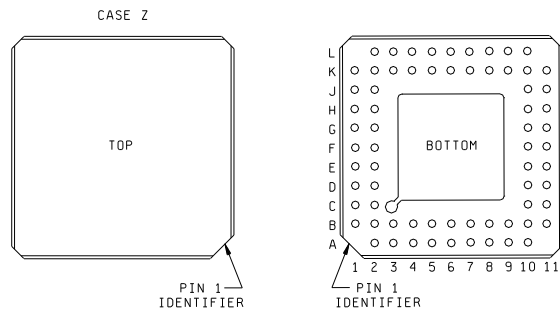


FIGURE 2. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-85010
		REVISION LEVEL C	SHEET 12



Case outline Z

Symbol	Location	Symbol	Location	Symbol	Location
$V_{CC}, V_{CC}$	F1, F11	A16/S3	A2	RD/QSMD	A5
$V_{SS}, V_{SS}$	L6, A6	AD15	B1	ARDY	B9
Reset	B8	AD14	C1	SRDY	C11
X1, X2	B7, A7	AD13	D1	LOCK	D10
CLKOUT	A8	AD12	E1	S0	A10
RES	L5	AD11	F2	S1	B10
TEST	D11	AD10	G2	S2	A9
TMR IN 0	L3	AD9	H2	HOLD	C10
TMR IN 1	K3	AD8	J2	(input)	
TMR OUT 0	L4	AD7	B2	HLDA	B11
TMR OUT 1	K4	AD6	C2	(output)	
DRQ0	L2	AD5	D2	UCS	L10
DRQ1	K2	AD4	E2	LCS	K9
NM1	E10	AD3	G1	MCS0-3	J10, J11, K10, K11
INT0, INT1	E11, F10	AD2	H1	PCS0	K5
INTA2/TNTA0	G10	AD1	J1	PCS1-4	K6, L7, K7, L8
INT3/TNTA1	G11	AD0	K1	PCS5/A1	K8
A19/S6	B4	BRE/S7	A4	PCS6/A2	L9
A18/S5	A3	ALE/QS0	B6	DT/R	H10
A17/S4	B3	WR/QS1	B5	DEN	H11

FIGURE 2. Terminal connections - Continued.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
13

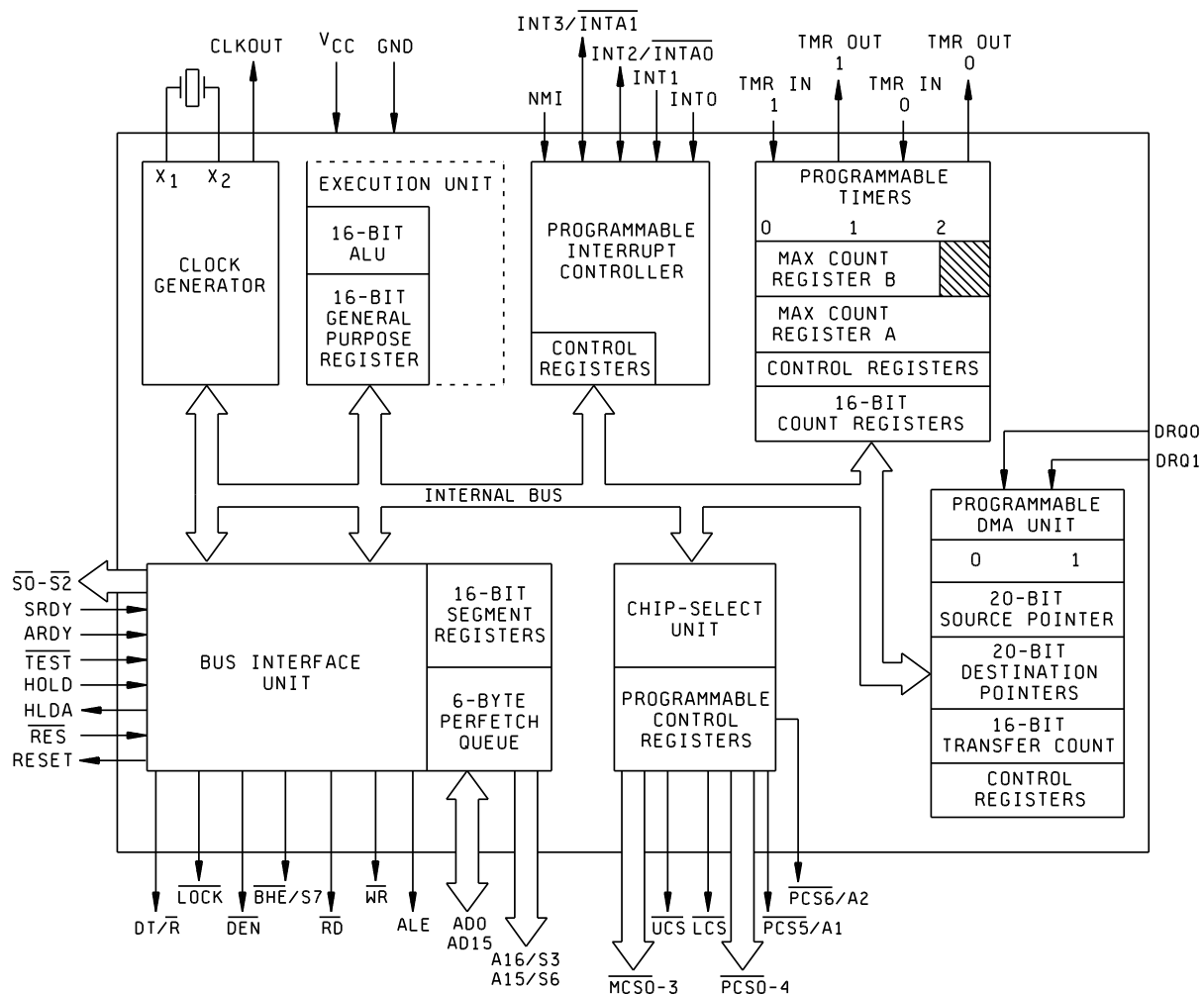


FIGURE 3. Functional block diagram.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
14

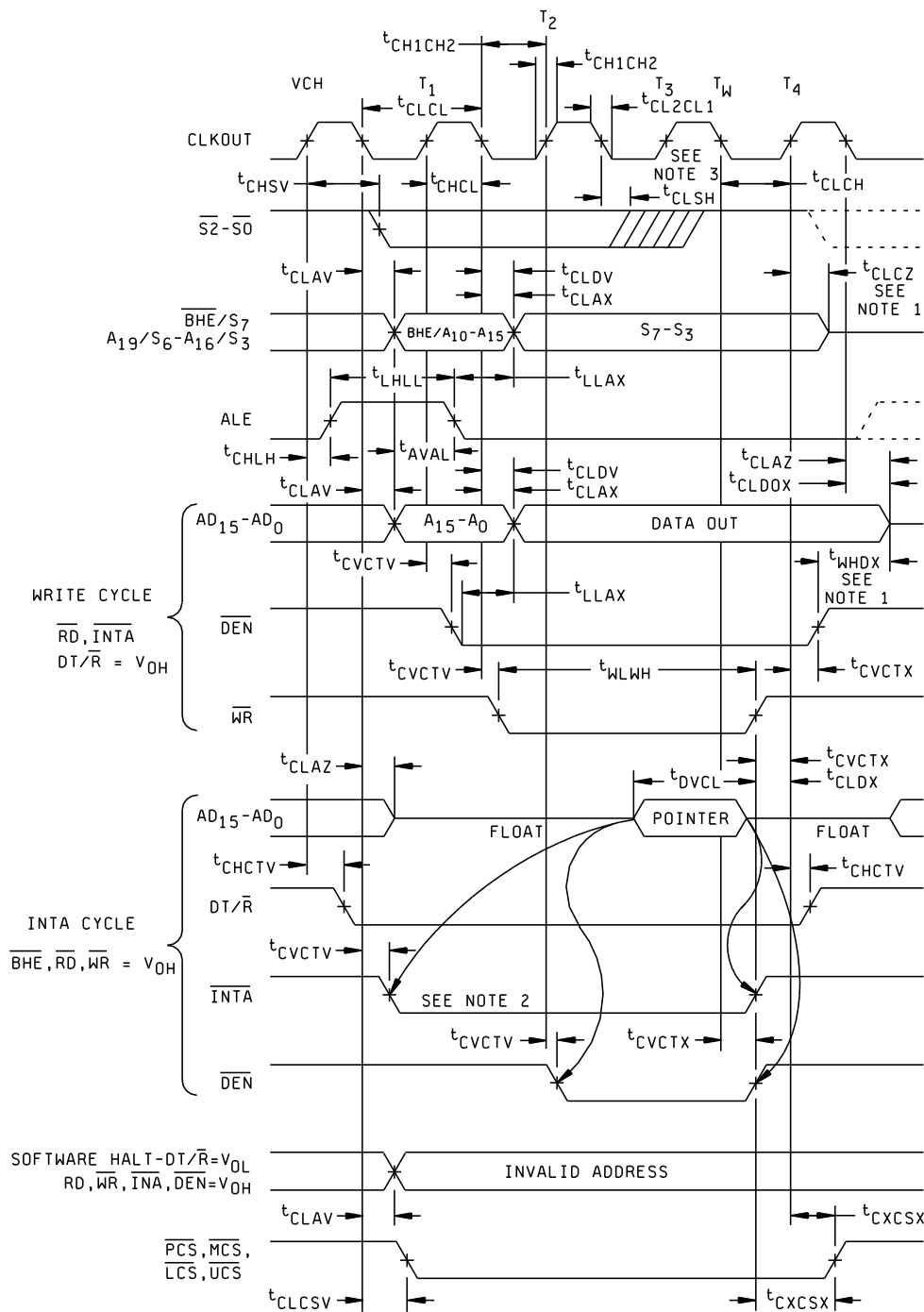


FIGURE 4. Timing waveforms.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
**C**

SHEET  
15



- FIGURE 4. Timing waveforms - Continued.

SHEET 16

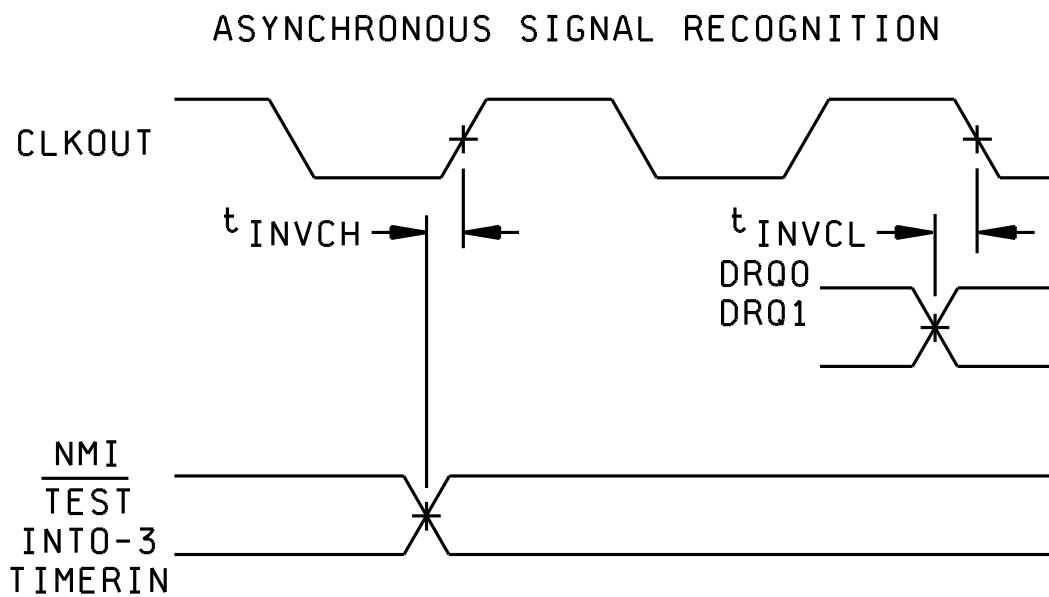
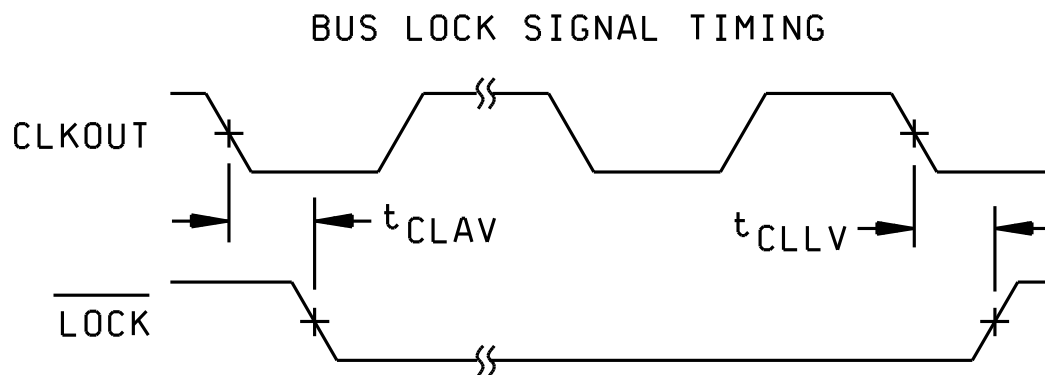


FIGURE 4. Timing waveforms - Continued.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
17

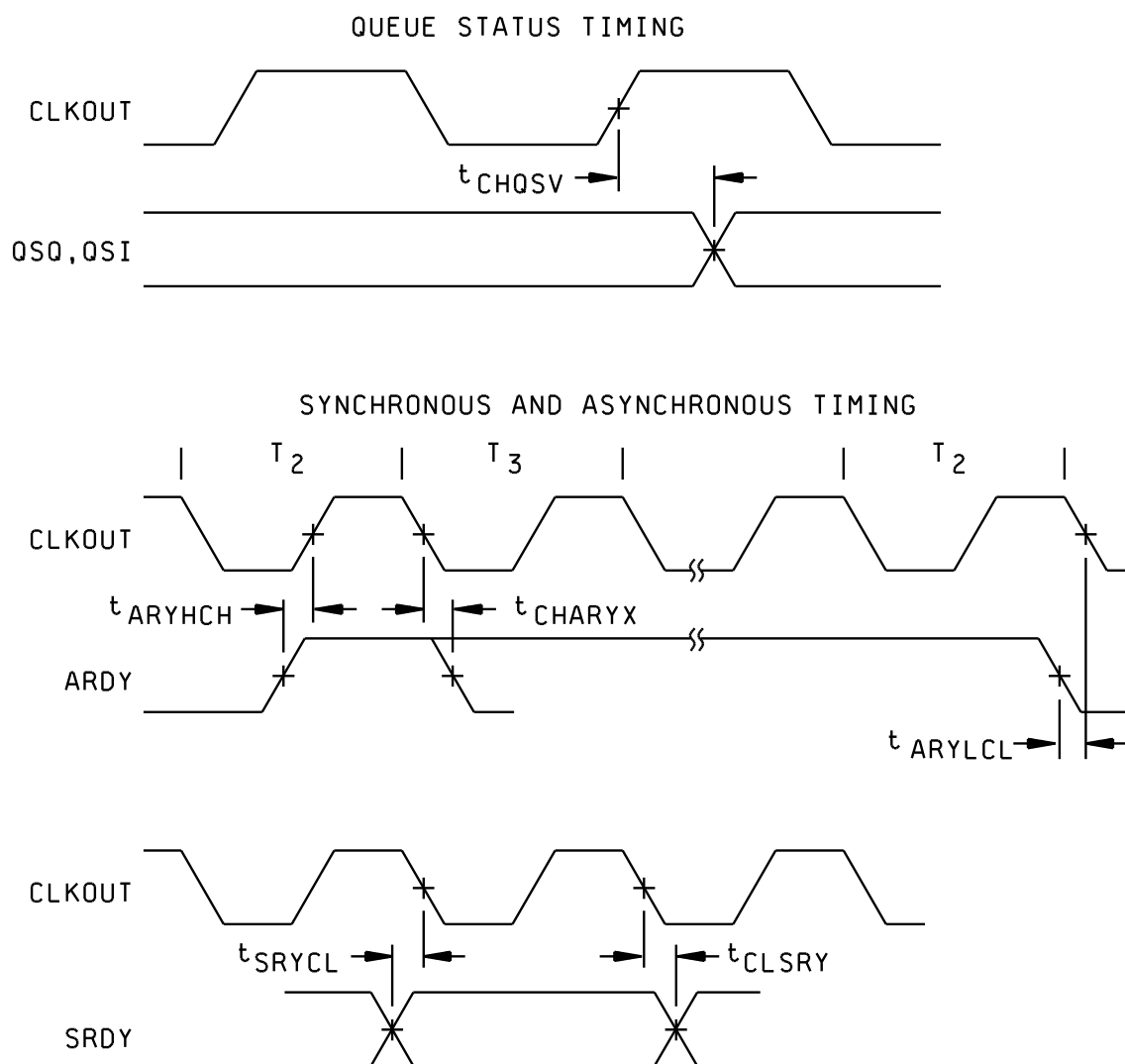


FIGURE 4. Timing waveforms - Continued.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
18

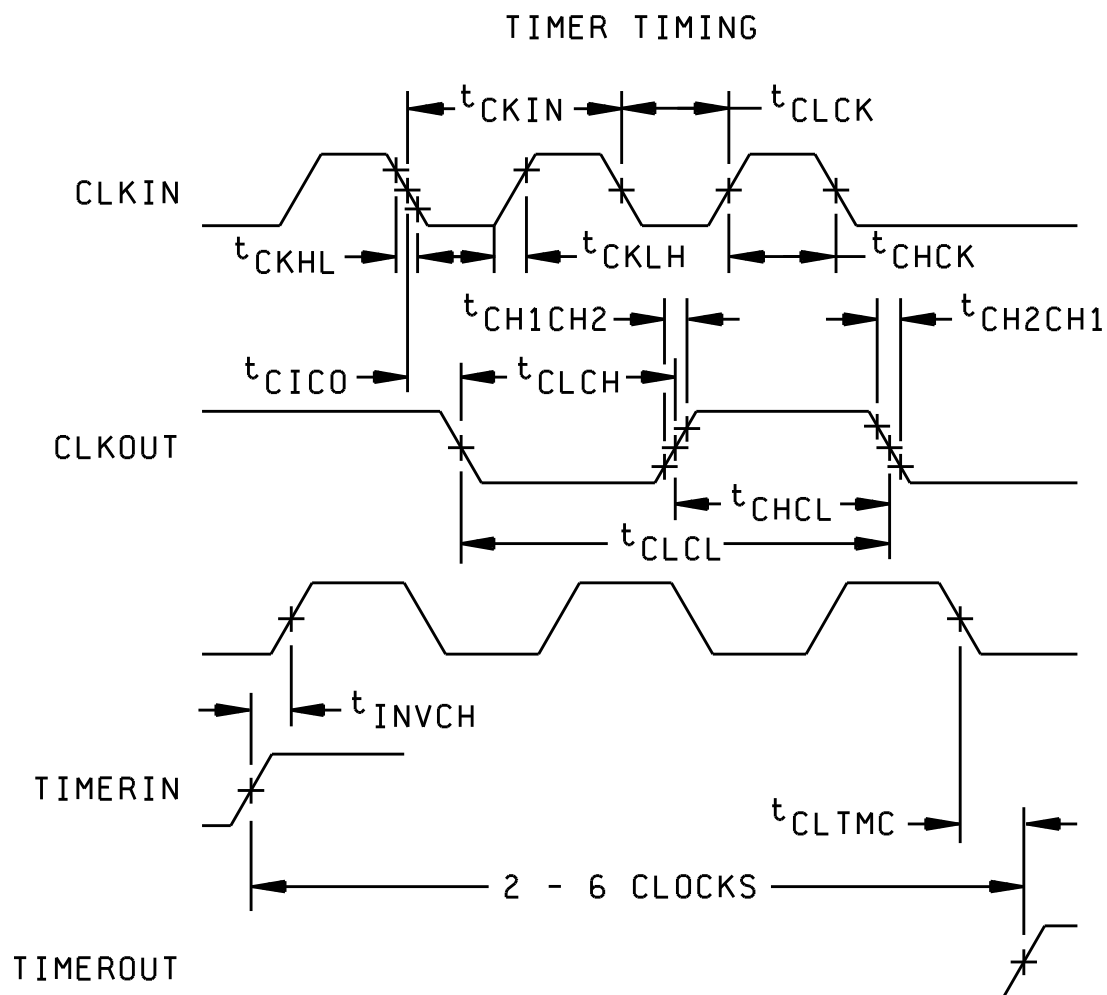


FIGURE 4. Timing waveforms - Continued.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
19

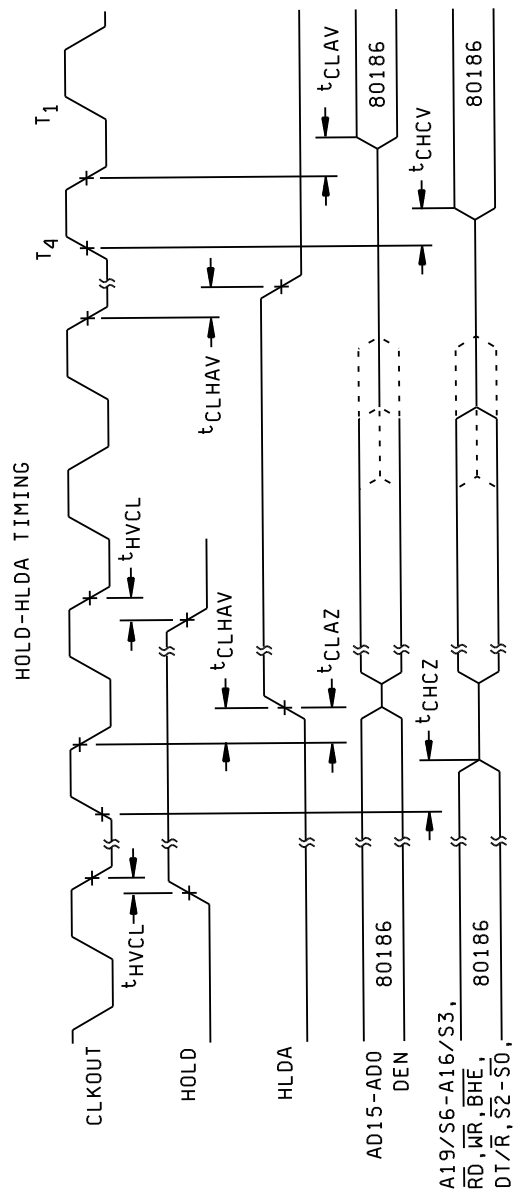


FIGURE 4. Timing waveforms - Continued.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
20

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.7 herein).
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

##### 4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$  and  $C_{IO}$  measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.
- d. Subgroups 7 and 8, functional testing shall include verification of instruction set (see table III).

<p style="text-align: center;"><b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</p>	SIZE <b>A</b>		5962-85010
		REVISION LEVEL C	SHEET 21

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8(+125° C), 10

\* PDA applies to subgroup 1.

#### 4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.7 herein).
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted method 1005 of MIL-STD-883.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
22

TABLE III. Instruction set summary.

Function	Format	Clock cycles	Comments
<b>DATA TRANSFER</b> MOV = Move:			
Register to register/memory	1 0 0 0 1 0 0 w    mod reg    r/m	1/12	
Register/memory to register	1 0 0 0 1 0 1 w    mod reg    r/m	2/9	
Immediate to register/memory	1 1 0 0 0 1 1 w    mod reg    r/m    data    data if W = 1	12-13	8/16-bit
Immediate to register	1 0 1 1 w    reg    data    data if W = 1	3-4	8/16-bit
Memory to accumulator	1 0 1 0 0 0 0 w    addr-low    addr-high	9	
Accumulator to memory	1 0 1 0 0 0 1 w    addr-low    addr-high	8	
Register/memory to segment register	1 0 0 0 1 1 1 0    mod 0 reg r/m	2/9	
Segment register to register/memory	1 0 0 0 1 1 0 0    mod 0 reg r/m	2/11	
PUSH = Push:			
Memory	1 1 1 1 1 1 1 1    mod 1 1 0    r/m	16	
Register	0 1 0 1 0    reg	10	
Segment register	0 0 0 reg 1 1 0	9	
Immediate	0 1 1 0 1 0 s 0    data    data if s = 0	10	
PUSHA = Push All	0 1 1 0 0 0 0 0		
POP = Pop:			
Memory	1 0 0 0 1 1 1 1    mod 0 0 0    r/m	20	
Register	0 1 0 1 1    reg	10	
Segment register	0 0 0 reg 1 1 1    (reg ≠ 01)	8	
POPA = Pop All	0 1 1 0 0 0 0 1	51	
XCHG = Exchange:			
Register/memory with register	1 0 0 0 0 1 1 w    mod reg    r/m	4/17	
Register with accumulator	1 0 0 1 0    reg	3	
IN = Input from:			
Fixed port	1 1 1 0 0 1 0 w    port	10	
Variable port	1 1 1 0 1 1 0 w	8	

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
23

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments				
OUT = Output to:							
Fixed port	<table><tr><td>1 1 1 0 0 1 1 w</td><td>port</td></tr></table>	1 1 1 0 0 1 1 w	port	9	8/16-bit		
1 1 1 0 0 1 1 w	port						
Variable port	<table><tr><td>1 1 1 0 1 1 1</td></tr></table>	1 1 1 0 1 1 1	7				
1 1 1 0 1 1 1							
XLAT = Translate byte to AL	<table><tr><td>1 1 0 1 0 1 1 1</td></tr></table>	1 1 0 1 0 1 1 1	11				
1 1 0 1 0 1 1 1							
LEA = Load EA to register	<table><tr><td>1 0 0 0 1 1 0 1</td><td>mod reg</td><td>r/m</td></tr></table>	1 0 0 0 1 1 0 1	mod reg	r/m		6	
1 0 0 0 1 1 0 1	mod reg	r/m					
LDS = Load pointer to DS	<table><tr><td>1 1 0 0 0 1 0 1</td><td>mod reg</td><td>r/m</td><td>(mod ≠ 11)</td></tr></table>	1 1 0 0 0 1 0 1	mod reg	r/m		(mod ≠ 11)	18
1 1 0 0 0 1 0 1	mod reg	r/m	(mod ≠ 11)				
LES = Load pointer to ES	<table><tr><td>1 1 0 0 0 1 0 0</td><td>mod reg</td><td>r/m</td><td>(mod ≠ 11)</td></tr></table>	1 1 0 0 0 1 0 0	mod reg	r/m		(mod ≠ 11)	18
1 1 0 0 0 1 0 0	mod reg	r/m	(mod ≠ 11)				
LAHF = Load AH with flags	<table><tr><td>1 0 0 1 1 1 1 1</td></tr></table>	1 0 0 1 1 1 1 1	2				
1 0 0 1 1 1 1 1							
SAHF = Store AH into flags	<table><tr><td>1 0 0 1 1 1 1 0</td></tr></table>	1 0 0 1 1 1 1 0	3				
1 0 0 1 1 1 1 0							
PUSHF = Push flags	<table><tr><td>1 0 0 1 1 1 0 0</td></tr></table>	1 0 0 1 1 1 0 0	9				
1 0 0 1 1 1 0 0							
POPF = Pop flags	<table><tr><td>1 0 0 1 1 1 0 1</td></tr></table>	1 0 0 1 1 1 0 1	8				
1 0 0 1 1 1 0 1							
SEGMENT = Segment Override:		2					
CS	<table><tr><td>0 0 1 0 1 1 1 0</td></tr></table>	0 0 1 0 1 1 1 0	2				
0 0 1 0 1 1 1 0							
DS	<table><tr><td>0 0 1 1 0 1 1 0</td></tr></table>	0 0 1 1 0 1 1 0	2				
0 0 1 1 0 1 1 0							
ES	<table><tr><td>0 0 1 0 0 1 1 0</td></tr></table>	0 0 1 0 0 1 1 0	2				
0 0 1 0 0 1 1 0							
ARITHMETIC							
ADD = Add:							
Reg/memory with register to either	<table><tr><td>0 0 0 0 0 0 d w</td><td>mod reg</td><td>r/m</td></tr></table>	0 0 0 0 0 0 d w	mod reg	r/m	3/10		
0 0 0 0 0 0 d w	mod reg	r/m					
Immediate to register/memory	<table><tr><td>1 0 0 0 0 0 s w</td><td>mod 0 0 0</td><td>r/m</td><td>data</td><td>data if s w = 01</td></tr></table>	1 0 0 0 0 0 s w	mod 0 0 0	r/m	data	data if s w = 01	4/16
1 0 0 0 0 0 s w	mod 0 0 0	r/m	data	data if s w = 01			
Immediate to accumulator	<table><tr><td>0 0 0 0 0 1 0 w</td><td>data</td><td>data if w = 1</td></tr></table>	0 0 0 0 0 1 0 w	data	data if w = 1	3/4		
0 0 0 0 0 1 0 w	data	data if w = 1					
ADC = Add with carry:							
Reg/memory with register to either	<table><tr><td>0 0 0 1 0 0 d w</td><td>mod reg</td><td>r/m</td></tr></table>	0 0 0 1 0 0 d w	mod reg	r/m	3/10		
0 0 0 1 0 0 d w	mod reg	r/m					
Immediate to register/memory	<table><tr><td>1 0 0 0 0 0 s w</td><td>mod 0 1 0</td><td>r/m</td><td>data</td><td>data if s w = 01</td></tr></table>	1 0 0 0 0 0 s w	mod 0 1 0	r/m	data	data if s w = 01	4/16
1 0 0 0 0 0 s w	mod 0 1 0	r/m	data	data if s w = 01			
Immediate to accumulator	<table><tr><td>0 0 0 1 0 1 0 w</td><td>data</td><td>data if w = 1</td></tr></table>	0 0 0 1 0 1 0 w	data	data if w = 1	3/4		
0 0 0 1 0 1 0 w	data	data if w = 1					
INC = Increment:							
Register/memory	<table><tr><td>1 1 1 1 1 1 1 w</td><td>mod 0 0 0</td><td>r/m</td></tr></table>	1 1 1 1 1 1 1 w	mod 0 0 0	r/m	3/15		
1 1 1 1 1 1 1 w	mod 0 0 0	r/m					
Register	<table><tr><td>0 1 0 0 0 reg</td></tr></table>	0 1 0 0 0 reg	3				
0 1 0 0 0 reg							

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
24

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
Sub = Subtract:			
Reg/memory and register to either	0 0 1 0 1 0 d w    mod reg    r/m	3/10	8/16-bit
Immediate from register/memory	1 0 0 0 0 0 w    mod 1 0 1    r/m    data    data if s w = 01	4/16	
Immediate from accumulator	0 0 1 0 1 1 0 w    data    data if w = 1	3/4	
SSB = Subtract with borrow:			
Reg/memory and register to either	0 0 0 1 1 0 d w    mod reg    r/m	3/10	8/16-bit
Immediate from register/memory	1 0 0 0 0 0 s w    mod 0 1 1    r/m    data    data if s w = 01	4/16	
Immediate from accumulator	0 0 0 1 1 1 0 w    data    data if w = 1	3/4	
DEC = Decrement:			
Register/memory	1 1 1 1 1 1 1 w    mod 0 0 1    r/m	3/15	3
Register	0 1 0 0 1 reg		
CMP = Compare:			
Register/memory with register	0 0 1 1 1 0 1 w    mod reg    r/m	3/10	8/16-bit
Register with register/memory	0 0 1 1 1 0 0 w    mod reg    r/m	3/10	
Immediate with register/memory	1 0 0 0 0 0 s w    mod 1 1 1    r/m    data    data if s w = 01	3/10	
Immediate with accumulator	0 0 1 1 1 1 0 w    data    data if w = 1	3/4	
NEG = Change sign	1 1 1 1 0 1 1 w    mod 0 1 1    r/m	3	
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	8	
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	4	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	7	
DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1	4	
MUL = Multiply (unsigned):			
Register-Byte Register-Word Memory-Byte Memory-Word	1 1 1 1 0 1 1 w    mod 1 0 0    r/m	26-28 35-37 32-34 41-43	
IMUL = Integer multiply (signed):			
Register-Byte Register-Word Memory-Byte Memory-Word	1 1 1 1 0 1 1 w    mod 1 0 1    r/m	25-28 34-37 31-34 40-43	

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-85010
		REVISION LEVEL C	SHEET 25

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
ARITHMETIC (Continued):			
IMUL = Integer immediate multiply (signed)	<div>0 1 1 0 1 0 s 1</div> <div>mod reg    r/m    dat    data if s = 0</div>	22-25/ 29-32	
DIV = Divide (unsigned):	<div>1 1 1 1 0 1 1 w</div> <div>mod 1 1 0    r/m</div>	29 38 35 44	
Register-Byte register-Word Memory-Byte Memory-Word			
IDIV = Integer divide (signed):	<div>1 1 1 1 0 1 1 w</div> <div>mod 1 1 1    r/m</div>	44-52 53-61 50-58 59-67	
Register-Byte Register-Word Memory-Byte Memory-Word			
AAM = ASCII adjust for multiply	<div>1 1 0 1 0 1 0 0</div> <div>0 0 0 0 1 0 1 0</div>	19	
AAD = ASCII adjust for divide	<div>1 1 0 1 0 1 0 1</div> <div>0 0 0 0 1 0 1 0</div>	15	
CBW = Convert byte to word	<div>1 0 0 1 1 0 0 0</div>	2	
CWD = Convert word to double word	<div>1 0 0 1 1 0 0 1</div>	4	
LOGIC			
Shift/rotate instructions:			
Register/memory by 1	<div>1 1 0 1 0 0 0 w</div> <div>mod TTT    r/m</div>	2/15	
Register/memory by CL	<div>1 1 0 1 0 0 1 w</div> <div>mod TTT    r/m</div>	5+n/ 17+n	
Register/memory by count	<div>1 1 0 0 0 0 0 w</div> <div>mod TTT    r/m    count</div>	5+n/ 17+n	
<div>TTT Instruction</div> <div>0 0 0    ROL</div> <div>0 0 1    ROR</div> <div>0 1 0    RCL</div> <div>0 1 1    RCR</div> <div>1 0 0    SHL/SAL</div> <div>1 0 1    SHR</div> <div>1 1 1    SAR</div>			

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
26

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments				
AND = And:							
Reg/memory and register to either	<table><tr><td>0 0 1 0 0 0 d w</td><td>mod reg</td><td>r/m</td></tr></table>	0 0 1 0 0 0 d w	mod reg	r/m	3/10	8/16-bit	
0 0 1 0 0 0 d w	mod reg	r/m					
Immediate to register/memory	<table><tr><td>1 0 0 0 0 0 w</td><td>mod 1 0 0</td><td>r/m</td><td>data</td><td>data if w = 1</td></tr></table>	1 0 0 0 0 0 w	mod 1 0 0	r/m	data		data if w = 1
1 0 0 0 0 0 w	mod 1 0 0	r/m	data	data if w = 1			
Immediate to accumulator	<table><tr><td>0 0 1 0 0 1 w</td><td>data</td><td>data if w = 1</td></tr></table>	0 0 1 0 0 1 w	data	data if w = 1	3/4		
0 0 1 0 0 1 w	data	data if w = 1					
TEST = And function to flags, no result:							
Register/memory and register	<table><tr><td>1 0 0 0 0 1 w</td><td>mod reg</td><td>r/m</td></tr></table>	1 0 0 0 0 1 w	mod reg	r/m	3/10	8/16-bit	
1 0 0 0 0 1 w	mod reg	r/m					
Immediate data and register/memory	<table><tr><td>1 1 1 1 0 1 w</td><td>mod 0 0 0</td><td>r/m</td><td>data</td><td>data if w = 1</td></tr></table>	1 1 1 1 0 1 w	mod 0 0 0	r/m	data		data if w = 1
1 1 1 1 0 1 w	mod 0 0 0	r/m	data	data if w = 1			
Immediate data and accumulator	<table><tr><td>1 0 1 0 1 0 w</td><td>data</td><td>data if w = 1</td></tr></table>	1 0 1 0 1 0 w	data	data if w = 1	3/4		
1 0 1 0 1 0 w	data	data if w = 1					
OR = Or:							
Reg/memory and register to either	<table><tr><td>0 0 0 0 1 0 d w</td><td>mod reg</td><td>r/m</td></tr></table>	0 0 0 0 1 0 d w	mod reg	r/m	3/10	8/16-bit	
0 0 0 0 1 0 d w	mod reg	r/m					
Immediate to register/memory	<table><tr><td>1 0 0 0 0 0 w</td><td>mod 0 0 1</td><td>r/m</td><td>data</td><td>data if w = 1</td></tr></table>	1 0 0 0 0 0 w	mod 0 0 1	r/m	data		data if w = 1
1 0 0 0 0 0 w	mod 0 0 1	r/m	data	data if w = 1			
Immediate to accumulator	<table><tr><td>0 0 0 0 1 1 w</td><td>data</td><td>data if w = 1</td></tr></table>	0 0 0 0 1 1 w	data	data if w = 1	3/4		
0 0 0 0 1 1 w	data	data if w = 1					
XOR = Exclusive or:							
Reg/memory and register to either	<table><tr><td>0 0 1 1 0 0 d w</td><td>mod reg</td><td>r/m</td></tr></table>	0 0 1 1 0 0 d w	mod reg	r/m	3/10	8/16-bit	
0 0 1 1 0 0 d w	mod reg	r/m					
Immediate to register/memory	<table><tr><td>1 0 0 0 0 0 w</td><td>mod 1 1 0</td><td>r/m</td><td>data</td><td>data if w = 1</td></tr></table>	1 0 0 0 0 0 w	mod 1 1 0	r/m	data		data if w = 1
1 0 0 0 0 0 w	mod 1 1 0	r/m	data	data if w = 1			
Immediate to accumulator	<table><tr><td>0 0 1 1 0 1 w</td><td>data</td><td>data if w = 1</td></tr></table>	0 0 1 1 0 1 w	data	data if w = 1	3/4		
0 0 1 1 0 1 w	data	data if w = 1					
NOT = Invert register/memory	<table><tr><td>1 1 1 1 0 1 w</td><td>mod 0 1 0</td><td>r/m</td></tr></table>	1 1 1 1 0 1 w	mod 0 1 0	r/m	3		
1 1 1 1 0 1 w	mod 0 1 0	r/m					
STRING MANIPULATION:							
MOVS = Move byte/word	<table><tr><td>1 0 1 0 0 1 w</td></tr></table>	1 0 1 0 0 1 w	14				
1 0 1 0 0 1 w							
CMPS = Compar byte/word	<table><tr><td>1 0 1 0 0 1 w</td></tr></table>	1 0 1 0 0 1 w	22				
1 0 1 0 0 1 w							
SCAS = Scan byte/word	<table><tr><td>1 0 1 0 1 1 w</td></tr></table>	1 0 1 0 1 1 w	15				
1 0 1 0 1 1 w							
LODS = Load byte/wd to AL/AX	<table><tr><td>1 0 1 0 1 1 w</td></tr></table>	1 0 1 0 1 1 w	12				
1 0 1 0 1 1 w							
STOS = Store byte/wd from AL/A	<table><tr><td>1 0 1 0 1 0 w</td></tr></table>	1 0 1 0 1 0 w	10				
1 0 1 0 1 0 w							
INS = input byte/wd from DX port	<table><tr><td>0 1 1 0 1 1 w</td></tr></table>	0 1 1 0 1 1 w	14				
0 1 1 0 1 1 w							
OUTS = Output byte/wd to DX port	<table><tr><td>0 1 1 0 1 1 w</td></tr></table>	0 1 1 0 1 1 w	14				
0 1 1 0 1 1 w							

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
27

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments				
STRING MANIPULATION (Continued): Repeated by count in CX							
MOVS = Move string	<table><tr><td>1 1 1 1 0 0 1 0</td><td>1 0 1 0 0 1 0 w</td></tr></table>	1 1 1 1 0 0 1 0	1 0 1 0 0 1 0 w	8+8n			
1 1 1 1 0 0 1 0	1 0 1 0 0 1 0 w						
CMPS = Compare string	<table><tr><td>1 1 1 1 0 0 1 z</td><td>1 0 1 0 0 1 1 w</td></tr></table>	1 1 1 1 0 0 1 z	1 0 1 0 0 1 1 w	5+22n			
1 1 1 1 0 0 1 z	1 0 1 0 0 1 1 w						
SCAS = Scan string	<table><tr><td>1 1 1 1 0 0 1 z</td><td>1 0 1 0 1 1 1 w</td></tr></table>	1 1 1 1 0 0 1 z	1 0 1 0 1 1 1 w	5+15n			
1 1 1 1 0 0 1 z	1 0 1 0 1 1 1 w						
LODS = Load string	<table><tr><td>1 1 1 1 0 0 1 0</td><td>1 0 1 0 1 1 0 w</td></tr></table>	1 1 1 1 0 0 1 0	1 0 1 0 1 1 0 w	6+11n			
1 1 1 1 0 0 1 0	1 0 1 0 1 1 0 w						
STOS = Store string	<table><tr><td>1 1 1 1 0 0 1 0</td><td>1 0 1 0 1 0 1 w</td></tr></table>	1 1 1 1 0 0 1 0	1 0 1 0 1 0 1 w	6+9n			
1 1 1 1 0 0 1 0	1 0 1 0 1 0 1 w						
INS = Input string	<table><tr><td>1 1 1 1 0 0 1 0</td><td>0 1 1 0 1 1 0 w</td></tr></table>	1 1 1 1 0 0 1 0	0 1 1 0 1 1 0 w	8+8n			
1 1 1 1 0 0 1 0	0 1 1 0 1 1 0 w						
OUTS = Output str9ng	<table><tr><td>1 1 1 1 0 0 1 0</td><td>0 1 1 0 1 1 1 w</td></tr></table>	1 1 1 1 0 0 1 0	0 1 1 0 1 1 1 w	8+8n			
1 1 1 1 0 0 1 0	0 1 1 0 1 1 1 w						
CONTROL TRANSFER							
CALL = Call:							
Direct within segment	<table><tr><td>1 1 1 0 1 0 0 0</td><td>disp-low</td><td>disp-high</td></tr></table>	1 1 1 0 1 0 0 0	disp-low	disp-high	14		
1 1 1 0 1 0 0 0	disp-low	disp-high					
Register/memory indirect within segment	<table><tr><td>1 1 1 1 1 1 1 1</td><td>mod 0 1 0</td><td>r/m</td></tr></table>	1 1 1 1 1 1 1 1	mod 0 1 0	r/m	13/19		
1 1 1 1 1 1 1 1	mod 0 1 0	r/m					
Direct intersegment	<table><tr><td>1 0 0 1 1 0 1 0</td><td>segment offset</td></tr><tr><td></td><td>segment selector</td></tr></table>	1 0 0 1 1 0 1 0	segment offset		segment selector	23	
1 0 0 1 1 0 1 0	segment offset						
	segment selector						
Indirect intersegment	<table><tr><td>1 1 1 1 1 1 1 1</td><td>mod 0 1 1</td><td>r/m</td></tr></table>	1 1 1 1 1 1 1 1	mod 0 1 1	r/m	38		
1 1 1 1 1 1 1 1	mod 0 1 1	r/m					
JMP = Unconditional jump:							
Short/long	<table><tr><td>1 1 1 0 1 0 1 1</td><td>disp-low</td></tr></table>	1 1 1 0 1 0 1 1	disp-low	13			
1 1 1 0 1 0 1 1	disp-low						
Direct within segment	<table><tr><td>1 1 1 0 1 0 0 1</td><td>disp-low</td><td>disp-high</td></tr></table>	1 1 1 0 1 0 0 1	disp-low	disp-high	13		
1 1 1 0 1 0 0 1	disp-low	disp-high					
Register/memory indirect within segment	<table><tr><td>1 1 1 1 1 1 1 1</td><td>mod 1 0 0</td><td>r/m</td></tr></table>	1 1 1 1 1 1 1 1	mod 1 0 0	r/m	11/17		
1 1 1 1 1 1 1 1	mod 1 0 0	r/m					
Direct intersegment	<table><tr><td>1 1 1 0 1 0 1 0</td><td>segment offset</td></tr><tr><td></td><td>segment selector</td></tr></table>	1 1 1 0 1 0 1 0	segment offset		segment selector	13	
1 1 1 0 1 0 1 0	segment offset						
	segment selector						
Indirect intersegment	<table><tr><td>1 1 1 1 1 1 1 1</td><td>mod 1 0 1</td><td>r/m</td></tr></table>	1 1 1 1 1 1 1 1	mod 1 0 1	r/m	26		
1 1 1 1 1 1 1 1	mod 1 0 1	r/m					
RET = Return from CALL:							
Within segment	<table><tr><td>1 1 0 0 0 0 1 1</td></tr></table>	1 1 0 0 0 0 1 1	16				
1 1 0 0 0 0 1 1							
Within seg adding immed to SP	<table><tr><td>1 1 0 0 0 1 0</td><td>data-low</td><td>data-high</td></tr></table>	1 1 0 0 0 1 0	data-low	data-high	18		
1 1 0 0 0 1 0	data-low	data-high					
Intersegment	<table><tr><td>1 1 0 0 1 0 1 1</td></tr></table>	1 1 0 0 1 0 1 1	22				
1 1 0 0 1 0 1 1							
Intersegment adding immediate to SP	<table><tr><td>1 1 0 0 1 0 1 0</td><td>data-low</td><td>data-high</td></tr></table>	1 1 0 0 1 0 1 0	data-low	data-high	25		
1 1 0 0 1 0 1 0	data-low	data-high					

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5962-85010

REVISION LEVEL  
C

SHEET  
28

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
CONTROL TRANSFER (Continued):			
JE/JZ = Jump on equal zero	0 1 1 1 0 1 0 0    disp	4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0    disp	4/13	
JLE/JNG = Jump on less or equal/ not greater	0 1 1 1 1 1 1 0    disp	4/13	
JB/JNAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0    disp	4/13	
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0    disp	4/13	
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0    disp	4/13	
JO = Jump on overflow	0 1 1 1 0 0 0 0    disp	4/13	
JS = Jump on sign	0 1 1 1 1 0 0 0    disp	4/13	
JNE/JNZ = Jump on not equal/ not zero	0 1 1 1 0 1 0 1    disp	4/13	
JNL/JGE = Jump on not less/ greater or equal	0 1 1 1 1 1 0 1    disp	4/13	
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1    disp	4/13	
JNB/JAE = Jump on not below/ above or equal	0 1 1 1 0 0 1 1    disp	4/13	
JNBE/JA = Jump on not below/ or equal/above	0 1 1 1 0 1 1 1    disp	4/13	
JNP/JPO = Jump on not par/par odd	0 1 1 1 1 0 1 1    disp	4/13	
JNO = Jump on not overflow	0 1 1 1 0 0 0 1    disp	4/13	
JNS = Jump on not sign	0 1 1 1 1 0 0 1    disp	4/13	
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1    disp	5/15	LOOP not taken/LOOP taken
LOOP = Loop CX times	1 1 1 0 0 0 1 0    disp	6/16	
LOOPZ/LOOPE = Loop while zero/ equal	1 1 1 0 0 0 0 1    disp	6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	1 1 1 0 0 0 0 0    disp	6/16	

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**A**

5962-85010

REVISION LEVEL  
C

SHEET  
29

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
ENTER = Enter procedure L = 0 L = 1 L > 1	<div>1 1 0 0 1 0 0 0</div> <div>data-low      data-high      L</div>	15 25 22+16 (n-1)	
LEAVE = Leave procedure	<div>1 1 0 0 1 0 0 1</div>	8	
INT = Interrupt: Type specified	<div>1 1 0 0 1 1 0 1</div> <div>type</div>	47	
Type 3	<div>1 1 0 0 1 1 0 0</div>	45	
INTO = Interrupt on overflow	<div>1 1 0 0 1 1 1 0</div>	48/4	if INT. taken/ if INT. not taken
IRET = Interrupt return	<div>1 1 0 0 1 1 1 1</div>	28	
BOUND = Detect value out of range	<div>0 1 1 0 0 0 1 0</div> <div>mod req      r/m</div>	33-35	
PROCESSOR CONTROL			
CLC = Clear carry	<div>1 1 1 1 1 0 0 0</div>	2	
CMC = Complement carry	<div>1 1 1 1 0 1 0 1</div>	2	
STC = Set carry	<div>1 1 1 1 1 0 0 1</div>	2	
CLD = Clear direction	<div>1 1 1 1 1 1 0 0</div>	2	
STD = Set direction	<div>1 1 1 1 1 1 0 1</div>	2	
CLI = Clear interrupt	<div>1 1 1 1 1 0 1 0</div>	2	
STI = Set interrupt	<div>1 1 1 1 1 0 1 1</div>	2	
HLT = Halt	<div>1 1 1 1 0 1 0 0</div>	2	
WAIT = Wait	<div>1 0 0 1 1 0 1 1</div>	6	if $\overline{\text{test}}$ = 0
LOCK = Bus lock prefix	<div>1 1 1 1 0 0 0 0</div>	2	
ESC = Processor extension escape	<div>1 0 0 1 1 T T T</div> <div>mod LLL      r/m</div> <div>(TTT LLL are opcode to processor extension)</div>	6	

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SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
30

# NOTES:

The effective address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field

if mod = 00 then DISP = 0\*, disp-low and disp-high are absent

if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent

if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP

if r/m = 001 then EA = (BX) + (DI) + DISP

if r/m = 010 then EA = (BP) + (SI) + DISP

if r/m = 011 then EA = (BP) + (DI) + DISP

if r/m = 100 then EA = (SI) + DISP

if r/m = 101 then EA = (DI) + DISP

if r/m = 110 then EA = (BP) + DISP\*

if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

\*Except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

## SEGMENT OVERRIDE PREFIX

0	0	1	reg	1	1	0
---	---	---	-----	---	---	---

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

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SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
31

NOTES - Continued.

REG is assigned according to the following table:

16-Bit(w = 1)	8-Bit(w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

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SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
32

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Symbols, definitions, and functional descriptions. The symbols, definitions, and functional descriptions for this device shall be as follows:

Symbol	Name and function
V <sub>CC</sub>	System power: +5 volt power supply.
V <sub>SS</sub>	System ground.
RESET	Reset output indicates that the 80186 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the RES signal.
X1, X2	Crystal inputs, X1 and X2, provide an external connection for a fundamental mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock instead of a crystal. In this case, minimize the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	Clock output provides the system with a 50 percent duty cycle waveform. All device pin timings are specified relative to CLKOUT.
RES	System reset causes the 80186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80186 clock. The 80186 begins fetching instructions approximately 7 clock cycles after RES is returned HIGH. RES is required to be LOW for greater than 4 clock cycles and is internally synchronized. For proper initialization, the LOW-to-HIGH transition of RES must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt-trigger to facilitate power-on RES generation via an RC network. When RES occurs, the 80186 will drive the status lines to an inactive level for one clock, and then three-state them.

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MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
33

**TEST** TEST is examined by the WAIT instruction. If the TEST input is HIGH when "WAIT" execution begins, instruction execution will suspend. TEST will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80186 is waiting for TEST, interrupts will be serviced. The input is synchronized internally.

**TMR IN 0, TMR IN 1** Timer inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized.

**TMR OUT 0, TMR OUT 1** Timer outputs are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.

**DRQ0, DRQ1** DMA request is driven HIGH by an external device when it desires that a DMA channel (channel 0 or 1) perform a transfer. These signals are active HIGH, level-triggered, and internally synchronized.

**NMI** Non-maskable interrupt is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from a LOW to HIGH initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.

**INT0, INT1, INT2/INTA0, INT3/INTA1** Maskable interrupt requests can be requested by strobing one of these pins. When configured as inputs, these pins are active HIGH. Interrupt requests are synchronized internally. INT2 and INT3 may be configured via software to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge-or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When iRMX mode is selected, the function of these pins changes.

**A19/S6, A18/S5, A17/S4, A16/S3** Address bus outputs (16-19) and bus cycle status (3-6) reflect the four most significant address bits during  $T_1$ . These signals are active HIGH. During  $T_2$ ,  $T_3$ ,  $T_W$ , and  $T_4$ , status information is available on these lines as encoded below:

	Low	High
S6	Processor cycle	DMA cycle

S3, S4, and S5 are defined as LOW during  $T_2$ - $T_4$ .

**AD<sub>15</sub>-AD<sub>0</sub>** Address/data bus (0-15) signals constitute the time multiplexed memory or I/O address ( $T_1$ ) and data ( $T_2$ ,  $T_3$ ,  $T_W$ , and  $T_4$ ) bus. The bus is active HIGH.  $A_0$  is analogous to BHE for the lower byte of the data bus, pins  $D_7$  through  $D_0$ . It is LOW during  $T_1$  when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations.

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DEFENSE ELECTRONICS SUPPLY CENTER  
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SIZE  
**A**

5962-85010

REVISION LEVEL  
**C**

SHEET  
**34**

$\overline{\text{BHE}}/\text{S7}$

During  $T_1$  the bus high enable signal should be used to determine if data is to be enabled onto the most significant half of the data bus, pins  $D_{15}-D_8$ .  $\overline{\text{BHE}}$  is LOW during  $T_1$  for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the higher half of the bus. The S7 status information is available during  $T_2$ ,  $T_3$ , and  $T_4$ . S7 is logically equivalent to  $\overline{\text{BHE}}$ . The signal is active LOW, and is three-stated OFF during bus HOLD.

BHE and AO encodings		
BHE value	AO value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus ( $D_{15}-D_8$ )
1	0	Byte transfer on lower half of data bus ( $D_7-D_0$ )
1	1	Reserved

$\text{ALE}/\text{QS0}$

Address latch enable/queue status 0 is provided by the 80186 to latch the address into the address latches. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding  $T_1$  of the associated bus cycle. The trailing edge is generated off the CLKOUT rising edge in  $T_1$ . Note that ALE is never floated.

$\overline{\text{WR}}/\text{QS1}$

Write strobe/queue status 1 indicates that the data on the bus is to be written into a memory or an I/O device.  $\overline{\text{WR}}$  is active for  $T_2$ ,  $T_3$ , and  $T_W$  of any write cycle. It is active LOW, and floats during "HOLD." It is driven HIGH for one clock during reset, and then floated. When the 80186 is in queue status mode, the  $\text{ALE}/\text{QS0}$  and  $\overline{\text{WR}}/\text{QS1}$  pins provide information about processor instruction queue interaction.

QS1	QS2	Queue operation
0	0	No queue operation
0	1	First opcode byte fetched from the queue
1	1	Subsequent byte fetched from the queue
1	0	Empty the queue

$\overline{\text{RD}}/\text{QSMD}$

Read strobe indicates that the 80186 is performing a memory or I/O read cycle.  $\overline{\text{RD}}$  is active LOW for  $T_2$ ,  $T_3$ , and  $T_W$  of any read cycle. It is guaranteed not to go LOW in  $T_2$  until after the address bus is floated.  $\overline{\text{RD}}$  is active LOW, and floats during "HOLD."  $\overline{\text{RD}}$  is driven HIGH for one clock during reset, and then the output driver is floated. A weak internal pull-up mechanism on the  $\overline{\text{RD}}$  line holds it HIGH when the line is not driven. During RESET the pin is sampled to determine whether the 80186 should provide ALE,  $\overline{\text{WR}}$ , and  $\overline{\text{RD}}$ , or if the queue-status should be provided.  $\overline{\text{RD}}$  should be connected to GND to provide queue-status data.

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SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
35

**ARDY** Asynchronous ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input, and is active HIGH. Only the rising edge is internally synchronized by the 80186. This means that the falling edge of ARDY must be synchronized to the 80186 clock. If connected to  $V_{CC}$ , no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle.

**SRDY** Synchronous ready must be synchronized externally to the 80186. The use of SRDY provides a relaxed system-timing specification on the ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active HIGH. If this line is connected to  $V_{CC}$ , no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied LOW.

**LOCK** LOCK output indicates that other system bus masters are not to gain control of the system bus while LOCK is active LOW. The LOCK signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of the instruction following the LOCK prefix. No prefetches will occur while LOCK is asserted. LOCK is active LOW, is driven HIGH for one clock during RESET, and then floated. If unused, this line should be tied LOW.

**$\overline{S0}$ ,  $\overline{S1}$ ,  $\overline{S2}$**  Bus cycle status  $\overline{S0}$ - $\overline{S2}$  are encoded to provide bus-transaction information.

80186 bus cycle status information			
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus cycle initiated
0	0	0	Interrupt acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Read data from memory
1	1	0	Write data to memory
1	1	1	Passive (no bus cycle)

The status pins float during "HOLD."

$\overline{S2}$  may be used as a logical M/ $\overline{IO}$  indicator, and  $\overline{S1}$  as a DT/R indicator.

The status lines are driven HIGH for one clock during reset, and then floated until a bus cycle begins.

**HOLD (input)** **HLDA (output)** HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the 80186 clock. The 80186 will issue a HLDA (HIGH) in response to a HOLD request at the end of  $T_4$  or  $T_1$ . Simultaneous with the issuance of HLDA the 80186 will float the local bus and control lines. After HOLD is detected as being LOW, the 80186 will lower HLDA. When the 80186 needs to run another bus cycle, it will again drive the local bus and control lines.

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MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
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SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
36

$\overline{UCS}$	Upper memory chip select is an active LOW output whenever a memory reference is made to the defined upper portion (1K-256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{UCS}$ is software programmable.
$\overline{LCS}$	Lower memory chip select is active LOW whenever a memory reference is made to the defined lower portion (1K-256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{LCS}$ is software programmable.
$\overline{MCS0-3}$	Mid-range memory chip select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K-512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{MCS0-3}$ are software programmable.
$\overline{PCS0}$	Peripheral chip select signals 0-4 are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{PCS0-4}$ are software programmable.
$\overline{PCS1-4}$	
$\overline{PCS5/A1}$	Peripheral chip select 5 or latched $A_1$ may be programmed to provide a sixth peripheral chip select, or to provide an internally latched $A_1$ signal. The address range activating $\overline{PCS5}$ is software programmable. When programmed to provide latched $A_1$ , rather than $\overline{PCS5}$ , this pin will retain the previously latched value of $A_1$ during a bus HOLD. $A_1$ is active HIGH.
$\overline{PCS6/A2}$	Peripheral chip select 6 or latched $A_2$ may be programmed to provide a seventh peripheral chip select, or to provide an internally latched $A_2$ signal. The address range activating $\overline{PCS6}$ is software programmable. When programmed to provide latched $A_2$ , rather than $\overline{PCS6}$ , this pin will retain the previously latched value of $A_2$ during a bus HOLD. $A_2$ is active HIGH.
$\overline{DT/R}$	Data transmit/receive controls the direction of data flow through the external data bus transceiver. When LOW, data is transferred to the 80186. When HIGH the 80186 places write data on the data bus.
$\overline{DEN}$	Data enable is provided as a data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access. $\overline{DEN}$ is HIGH whenever $\overline{DT/R}$ changes state.

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
37

6.5 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.6 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.7) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number <sup>1/</sup>
8501001ZX	34649 34335	MG80186-8/B 80186/BZC
8501001YX	34649	MQ80186-8/B
8501002ZX	34649	MG80186-6/B 80186-6/BZC
8501002YX	34335	MQ80186-6/B

<sup>1/</sup> Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

Vendor name  
and address

34335

Advanced Micro Devices  
901 Thompson Place  
P.O. Box 3453  
Sunnyvale, CA 94081

34649

Intel Corporation  
3065 Bowers Avenue  
Santa Clara, CA 95051

**STANDARDIZED  
MILITARY DRAWING**  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

5962-85010

REVISION LEVEL  
C

SHEET  
38